

## REMARKS

Reconsideration of this application as amended is requested. By this amendment Applicant has canceled claims 1-5 and replaced them with new claims 6-9. Claims 6-9 are in the case.

The Examiner rejected claims 1-5 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description, stating that there is no support in the original specification for the claimed limitation of “the specific decoder supplementing the generic decoder in realtime.” Applicant has replaced claims 1-5 with new claims 6-9 that do not include the quoted language. Therefore claims 6-9 are deemed to comply with the written description requirement of 35 U.S.C. 112, first paragraph, rendering the Examiner’s rejection moot.

The Examiner further maintained the rejection of claims 1-5 under 35 U.S.C. 102(b) as being anticipated by Yang. Applicant respectfully traverses this conclusion by the Examiner.

In contradistinction to Applicant’s claimed invention Yang discloses a protocol analyzer, simulator and tester (PAST) for use in compatibility testing of CDMA mobile systems (CMS), PAST having a multi-processing kernel and multi-scenario handling to simulate more than one system simultaneously. The PAST architecture is used in testing protocol implementations of level N in the OSI reference model and has an upper layer interface (UT) accessible through a user task to provide stimuli to a system under test (SUT) and a lower layer interface (LT) acting as a communications interface with the SUT. Specifically the LT couples to a network interface using a custom layer 1 interface and has an interface controller at level 2 (PIC) for communicating between the level 1 network interface and the UT. The UT, such as an IBM compatible PC having an MS-DOS operating system, communicates with the LT via PDLs. Test data files are processed by the PDLs to provide stimuli to the SUT via the network interface, and result files are generated from the PDLs for data from the SUT. A display is included to

show results and provide a human visual interface. A user terminal is used to communicate with the UT to interact with the PAST.

Applicant recites in new claims 6 and 8, replacing claims 1-5 without the reversible connection limitation, a generic decoder into which a limited number of protocol descriptions are loaded, which descriptions are interpreted by the generic decoder during operation of the decoding device to convert coded data at an input into decoded data at an output. Then Applicant recites a specific decoder adapted to interpret a specific protocol. The Examiner first tries to equate Applicant's "generic decoder" with the PIC of Yang and erroneously states that the PDLs are loaded into the PIC, when in fact the PDLs exist in the PC. The PIC of Yang is not "adapted to interpret the protocol descriptions" as asserted by the Examiner. Then the Examiner equates Applicant's "specific decoder" with the UT of Yang, indicating that the PIC and PC are reversibly connected, which element is now recited in new claims 7 and 9. In fact the PIC is a peripheral controller that is compatible with the ISA bus and provides a communications interface between the PC and the outside world or SUT. Although the PIC has a microprocessor based system, there is no indication in Yang that the PC and PIC may be modified separately, i.e., they are not "reversibly connected." Yang's PIC merely serves as an interface and not as a decoder. There is no indication in Yang that a specific function of the PIC is overlaid with a corresponding function from the specific decoder or PC so that the PIC interprets, i.e., decodes coded data into decoded data, the corresponding function as part of the generic decoder as is recited by Applicant in claims 6 and 8.

Yang does not have the configuration where the generic decoder provides the interpretation of protocol descriptions to convert coded data into decoded data as recited by Applicant in claims 6 and 8, and where the recited specific decoder merely provides function overlays that relate to a specific protocol to the generic decoder. Yang shows a serial architecture where coded data from the network passes through the LT to the UT, and the UT does not merely provide overlays for processing by the LT. The UT is the device that actually decodes the coded data since the PIC in the LT is merely a communications interface and not a decoder. Thus new claims 6-9, claims 7

and 9 including the reversible connection between the two decoders, are deemed to be allowable as being neither anticipated nor rendered obvious to one of ordinary skill in the art by Yang.

In view of the foregoing amendment and remarks allowance of new claims 6-9 is urged, and such action and the issuance of this case are requested.

Respectfully submitted,

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